

DESIGN AND FABRICATION OF THE MICROCANTILEVER HEATER  
FOR RAPID CHEMICAL VAPOR DEPOSITION GRAPHENE SYNTHESIS

BY

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THESIS

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## **ABSTRACT**

This thesis presents the design and the fabrication process of the microcantilever heater for rapid chemical vapor deposition (CVD) graphene synthesis. Two types of 300 nm thick catalytic metals, copper and nickel, are integrated into the heater region ranging from 5 by 5  $\mu\text{m}$  to 20 by 12  $\mu\text{m}$  in size. The microcantilever heater is thermally actuated by Joule heating. The fabricated device is able to operate at the graphene synthesis temperature, ranging from 800°C to 1000°C, for longer than an hour without any degradation in functionality. To prevent electrical contact between the doped silicon device layer and the patterned catalytic metal, 200 nm of PECVD silicon nitride is deposited as a passivation layer. Raman spectroscopy measurements show that the temperature along the heater region is uniform with less than 5 % in difference. With rapid local heating and cooling of the fabricated microcantilever heater, the total graphene synthesis time is reduced by more than 90 % compared to conventional CVD. Using a nickel layered microcantilever heater, multilayer graphene was grown and analyzed with Raman spectroscopy. A detailed process flow of the microcantilever heater fabrication process and the device characterization results are explained in detail.

*This thesis is dedicated to my beloved family for their limitless love, sacrifice, and support.*

*Particularly to my father, who has been my lifetime advisor, for instilling the importance of  
education and for guiding me to achieve my dreams.*

## **ACKNOWLEDGMENTS**

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# CHAPTER 1

## INTRODUCTION

Graphene has drawn much attention in recent years with its fascinating electrical and mechanical properties [1] such as quantum electronic transport [2], a tunable bandgap, extremely high mobility, and outstanding thermal conductivity [3]. Many graphene synthesis methods have been developed in recent years. Initially, graphene was fabricated by the micromechanical cleaving of graphite, or the so called Scotch-tape method, which allowed the first isolated study of graphene properties [1]. Although this method provides high structural and electronic quality graphene that is sufficient for basic property studies, it is time consuming, unreliable, and most importantly, not suitable for large scale graphene production. The second graphene fabrication method is to reduce graphene oxide to graphene either by means of chemical or thermal annealing [4]. Graphene fabricated from this method has inconsistent thickness and is limited to tens of microns in size. Epitaxial growth of graphene on silicon carbide (SiC) gives high quality multilayer graphene, which can be patterned via standard lithographic procedures [5]. SiC reduces to graphene after a thermal treatment between 1250°C and 1450°C, and the number of grown graphene layers is temperature dependent [6]. However, graphene grown on SiC is hard to transfer to other substrates.

Recently, graphene has been grown on metal substrates by CVD [7-10]. The graphene CVD growth process gives a high quality graphene layer, which can be transferred to the desired substrate by etching the catalytic metal substrate. Since graphene is formed on the entire substrate metal surface, the CVD approach is suitable for large scale synthesis. Recently, 30 inch graphene films for transparent electrodes have been grown on flexible copper substrates

with a CVD roll-to-roll method [11]. The mechanism of CVD growth on nickel is based on precipitation [8]. Since the solubility of carbon in nickel is temperature dependent, by cooling the heated carbon and nickel solution, carbon atoms supersaturate and form a graphene layer on top of nickel. Different cooling rates lead to different segregation behaviors. With the rapid cooling rate, a finite amount of carbon can segregate at the surface and generate a uniform layer of graphene [7]. Unlike nickel, CVD graphene synthesis on a copper substrate is a self-limiting process due to the low carbon solubility in copper [9]. On copper, graphene is grown by a surface catalyzed process and only monolayer graphene is formed, independent of the synthesis time and substrate thickness.

Although the graphene CVD synthesis method is cost effective and suitable for large scale growth, the major shortcoming is its lengthy growth time, normally ranging from 2 hours to 3.5 hours [12]. However, the microcantilever heater can address this problem with rapid heating and cooling rates, which takes less than a few milliseconds to reach 1000°C and return to room temperature. The rapid cooling rate of the microcantilever heater suppresses the carbon segregation at metal grain boundaries, resulting in higher quality and more uniform formation of graphene. Using the microcantilever heater, the exact synthesis temperature can be controlled, thus the effect of the temperature to graphene synthesis can be closely monitored. This thesis explores the design and the detailed fabrication process of the microcantilever heater for rapid graphene CVD growth.

## CHAPTER 2

### CANTILEVER DESIGN

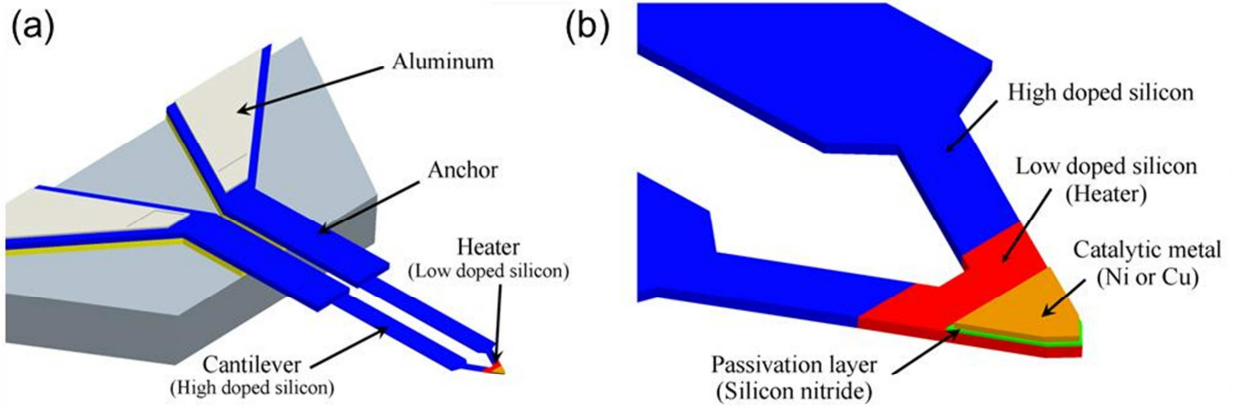
The design for microcantilever heater for rapid CVD graphene synthesis is based on the design for silicon AFM cantilevers having integrated solid-state heating elements which were originally designed for data storage [13, 14]. The legs of the cantilever are highly doped with phosphorus while the area at the free end is low doped with phosphorus to form the heater region. Passing current through the cantilever causes joule heating at the heater region and raises the heater temperature up to 1000°C, which is sufficient to synthesize graphene. The cantilever has a thermal time constant of 300  $\mu$ sec [15]. A similar cantilever design has been used for the CVD carbon nanotube (CNT) growth using a 10 nm thick iron film as a catalyst [16]. Based on the CNT growth study, it is assumed that the near field temperature surrounding the heater region is high enough to induce decomposition of the carbonaceous gases.

A 200 nm thick layer of plasma enhanced CVD (PECVD) silicon nitride is deposited on the silicon device layer to electrically isolate the catalytic metal layer and protect the device from the unwanted diffusion between the doped silicon device layer and the catalytic metal at high temperatures. The passivation layer is deposited at mixed frequency to minimize the surface stress. Silicon nitride is selected over silicon dioxide due to its higher thermal conductivity and slower etch rate in hydrofluoric acid (HF).

Figure 2.1 shows the proposed microcantilever heater. The key aspect of the cantilever is the patterned catalytic metal layer with a silicon nitride passivation layer at the free end of the cantilever. Two different catalytic metal substrates, copper and nickel, are patterned to compare and study the graphene growth on different materials. The catalytic metal layer should be thick

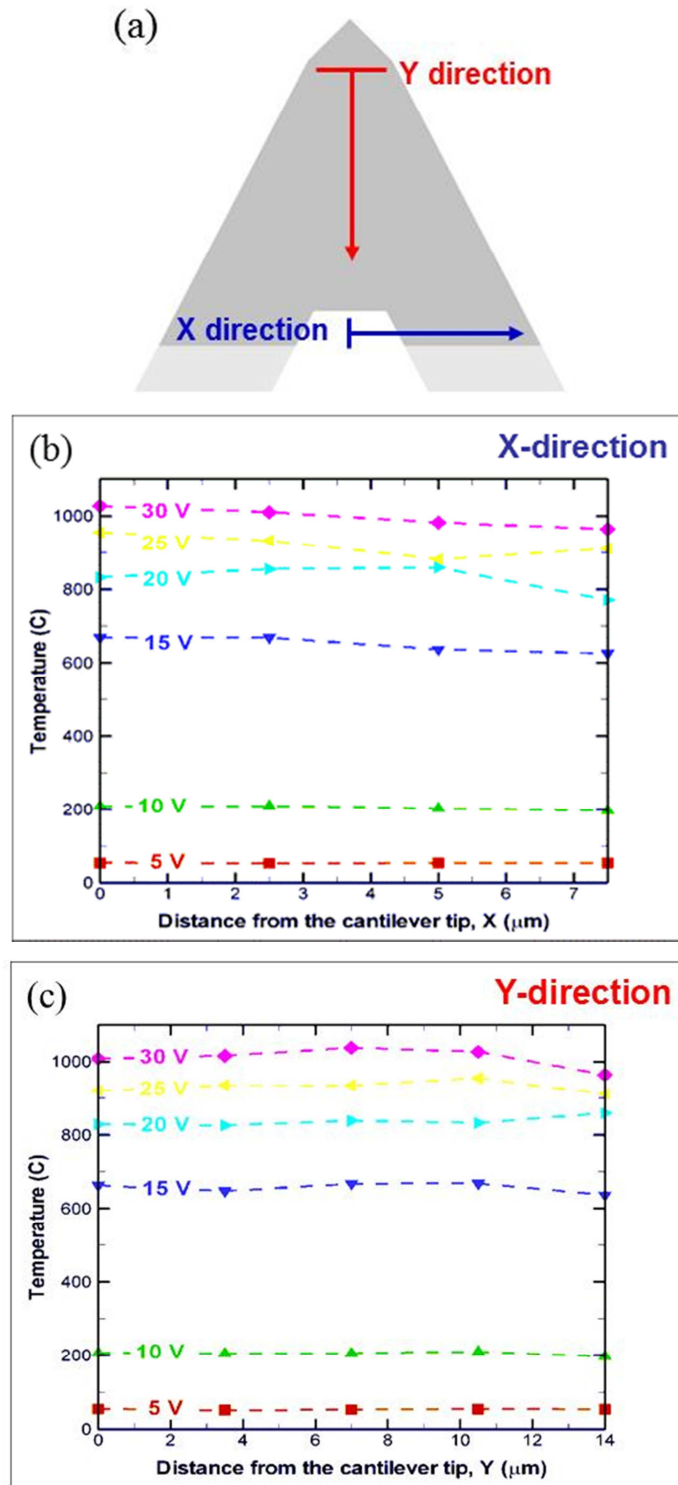


enough to avoid island formations that result in the growth of CNT instead of a uniform graphene film [8, 17]. For the continuous graphene growth, the devices are patterned with a 300 nm thick layer of either catalytic metal. A 10 nm chromium layer is added before the catalytic metal deposition to enhance the catalytic metal adhesion. The metal adhesion quality directly affects the yield of final devices. With poor adhesion quality, the silicon nitride passivation layer under the catalytic metal gets etched by HF during the final release process.



**Figure 2.1** Design of the microcantilever heater for rapid CVD graphene synthesis. a) Schematic of the entire cantilever. b) Detailed view of the heater region. The 200 nm silicon thick nitride passivation layer electrically isolates the doped silicon device layer from the catalytic metal layer at the heater region of the cantilever.

Figure 2.2 shows the temperature distribution across the heated AFM cantilever heater region measured using Raman spectroscopy. The spectroscopy measurements show that the temperature difference is less than 5 percent along both vertical and horizontal directions at 1000°C. Following the thermal mapping over the heater region, three different catalytic metal sizes are designed ranging from 5 by 5  $\mu\text{m}$  to 20 by 12  $\mu\text{m}$ , to better understand the effect of grain size on the growth of graphene.



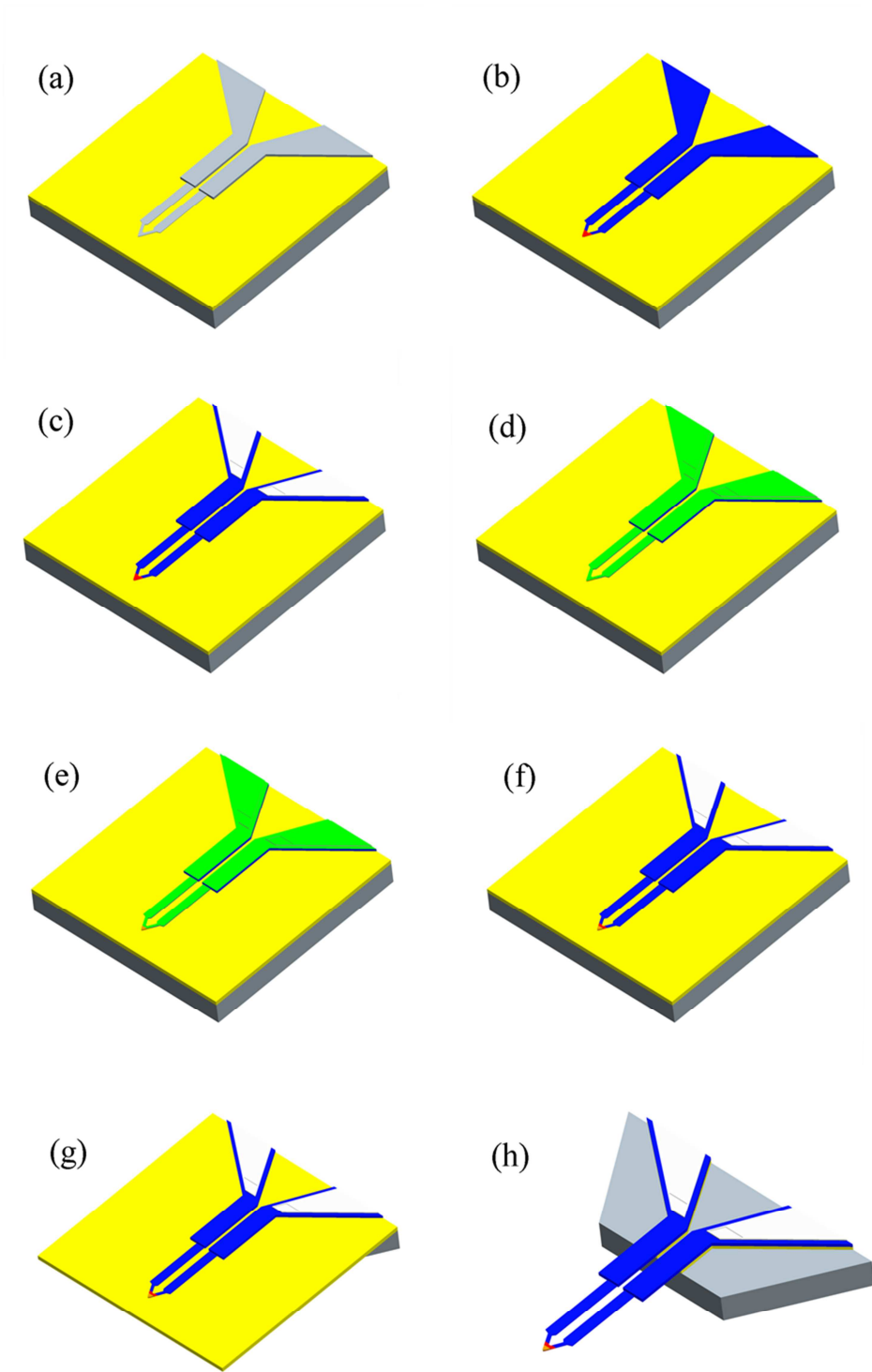
**Figure 2.2** Temperature distributions on the heated cantilever heater region. a) Schematic of the microcantilever heater region. b) Temperature distribution along the x-direction under different voltage inputs. c) Temperature distribution along the y-direction under different voltage inputs.

## CHAPTER 3

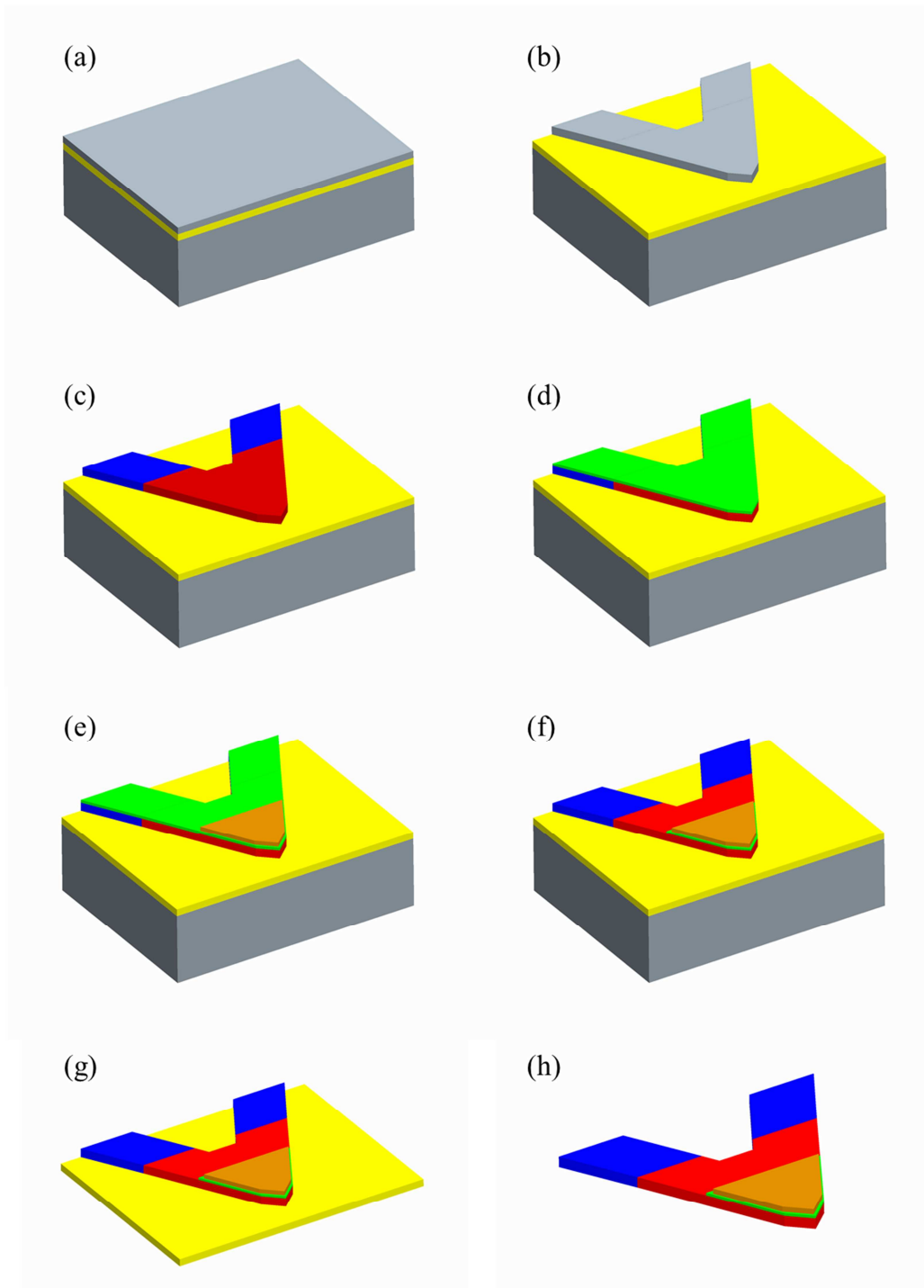
### FABRICATION PROCESS

The fabrication process of the microcantilever heater for rapid CVD graphene synthesis is explained in detail in this chapter. The device fabrication procedures are built upon an evolution of processing techniques first developed by IBM Zurich Research Laboratory groups [18]. These methods have been further progressed at Stanford University and Georgia Institute of Technology [13, 19]. Fabrication of the microcantilever heater follows five major processing steps; 1) Anchor and cantilever beam formation, 2) electrical activation, 3) metallization, 4) catalytic metal deposition and liftoff, 5) and backside through wafer etch and release. Figure 3.1 gives an overview of the entire fabrication process. Similarly, figure 3.2 shows the zoomed view of the cantilever free end in each fabrication step. All fabrication processes are carried out using facilities in the Micro-Nano-Mechanical Systems Laboratory (MNMS) and the Micro & Nanotechnology Laboratory (MNTL) at the University of Illinois Urbana-Champaign.

Four inch <100> silicon on insulator (SOI) wafer is used for the device fabrication with 5  $\mu\text{m}$  silicon device layer, 1  $\mu\text{m}$  silicon dioxide box layer, and 400  $\mu\text{m}$  silicon handle layer. The device layer has an intrinsic resistivity of 1-10  $\Omega\text{-cm}$ . Before the each fabrication step, the wafer is degreased via acetone-IPA-DI water clean and dehydration baked at 130°C for longer than 5 minutes.



**Figure 3.1** Overview of fabrication process showing the entire microcantilever heater structure. (a) Anchor and cantilever beam formation, (b) low dosage and high dosage phosphorous implantation, (c) metallization, (d) PECVD silicon nitride deposition, (e) catalytic metal deposition and liftoff, (f) silicon nitride etch, (g) backside through wafer etch, (h) final device release



**Figure 3.2** Overview of fabrication process zoomed in to highlight the catalytic metal and the passivation layer at the cantilever free end. (a) SOI wafer (b) anchor and cantilever beam formation (c) low dosage and high dosage phosphorus implantation, (d) PECVD silicon nitride deposition, (e) catalytic metal deposition and liftoff, (f) silicon nitride etch, (g) Backside through wafer etch, (h) final device release

### 3.1 Cantilever Formation

The first fabrication step is to pattern and etch the device layer to create the physical cantilever structure. Unlike the heated AFM cantilever, the graphene synthesis cantilever does not have a tip in the heater region. To thin the device layer to 1  $\mu\text{m}$ , the wafer is transferred to the STS ICP where a fluorine based BOSCH process etches the silicon device layer. A following photolithography step defines the cantilever, anchor, and base device structure into the photoresist. After the photoresist development and hard-baking, the wafer is once again transferred to STS ICP to etch remaining silicon device layer until the buried oxide layer is exposed. Unlike the heated AFM cantilever where the thicknesses of the cantilever structure and anchor / base region are different, the tip-less graphene growth cantilever has a uniform device layer thickness.

### 3.2 Ion Implantation and Diffusion

A silicon cantilever becomes electrically active by selectively masking, doping, and diffusing impurities into the silicon device layer. By selectively masking the cantilever, different resistivity regions can exist on the same cantilever. The implantation and diffusion process consists of two separate steps with different doping concentrations. Doping regions and doping concentration values are determined that 90% of the total cantilever resistance being generated in the heater region. Phosphorous was chosen over boron for implantation due to its higher resistivity at a given doping concentration. A higher resistivity throughout the device provides the efficient power delivery as well as the better heating and cooling efficiency.

In order to drive in the implanted impurities through the silicon device layer, the wafer is heated inside the annealing furnace. To prevent the dopant evaporation, a 300nm thick PECVD

oxide layer is deposited after the ion implantation and before the diffusion. The dopant drive in temperature for both low and high doping concentration diffusion steps is set to 1000°C.

The first low dosage implantation step is to create a uniform background resistivity for the entire cantilever and anchor. The heater region is masked during the following high dosage implantation step to maintain the high resistance. For the cantilever masking, a 2.7  $\mu\text{m}$  thick SC1827 photoresist film is used. After the ion implantation, the photoresist masking material is removed and a 300 nm thick PECVD oxide layer is deposited. To drive in implanted impurities, the wafer is introduced into the annealing furnace at 1000°C for 0.5 hours. The first implantation and diffusion step generates volumetric concentration of  $1\text{e}17$  atoms per cubic centimeter. Such volumetric concentration gives the heater region resistance value of 2 k $\Omega$ . After the diffusion step, a PECVD oxide layer is etched by buffered oxide etchant (BOE) for 3 minutes.

The second ion implantation is to electrically activate the legs and anchor with a high doping concentration. After the diffusion, the volumetric concentration of the legs and anchor is  $1\text{e}20$  atoms per cubic centimeters. Compared to the first implantation and diffusion step, it is harder to remove the photoresist masking material due to the higher ion bombardment energy during the implantation process. For the cleaning, 12 hours of acetone soak and 20 minutes of piranha clean is needed. After the wafer cleaning, a 300nm thick PECVD oxide film is deposited followed by the diffusion step at 1000°C for 2 hours. Once both sets of dopant implantation and diffusion steps are completed, the cantilever is electrically active and ready for the metal contact formation.

### 3.3 Electrical Contact Formation

The cantilever is electrically active and requires metal leads to connect the active cantilever structure to the base of the device. A 300 nm thick oxide layer from the previous diffusion step gives an electrical isolation between the silicon device layer and the metal leads. To establish an electrical contact between the cantilever and the metal leads, holes through an oxide layer are necessary. To generate these holes, an oxide layer is selectively masked with a SC1827 photoresist film and wet etched by BOE.

For the metal leads, a 1.5  $\mu\text{m}$  thick aluminum layer is evaporated using an e-beam evaporator. A relatively thick aluminum layer is desired since it gets attacked by HF during the final release step. A deposited aluminum layer is patterned with SC1827 and then etched using an aluminum etchant type A at 60°C for 5 to 8 minutes. Once the masking layer is cleaned, the cantilever resistance is measured. To further enhance the contact between the cantilever and the evaporated aluminum, a 30 minute vacuum annealing at a temperature of 400°C is completed. After this point, a piranha clean should be avoided since it attacks aluminum.

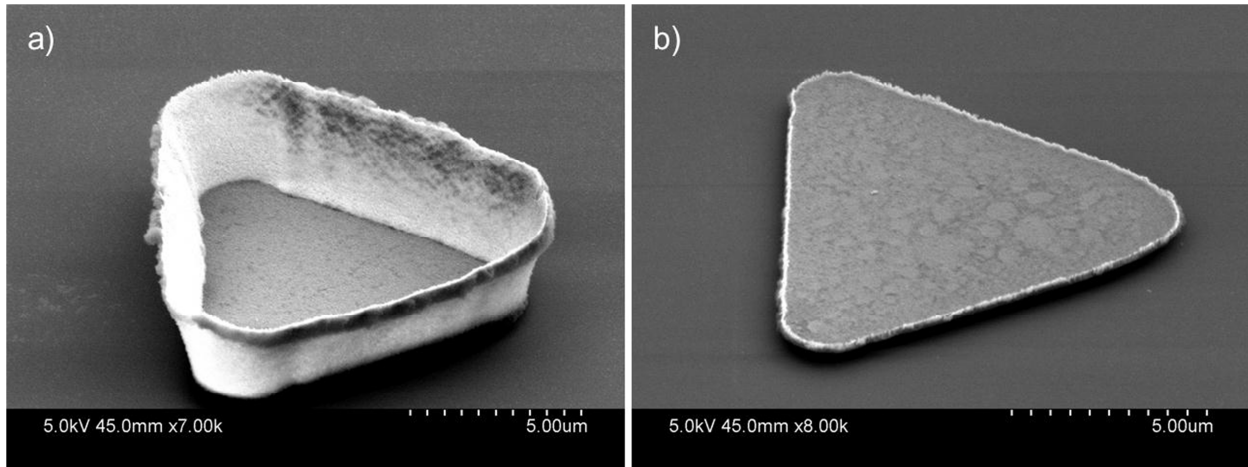
### 3.4 Catalytic Metal Deposition and Lift-off

At this point, the device is ready for the catalytic metal deposition and the liftoff process. A 300 nm thick oxide layer on top of the silicon device layer is etched using BOE. For the passivation layer, a 200 nm thick PECVD silicon nitride is deposited. To minimize the surface stress of the silicon nitride layer, a mixed frequency deposition recipe is used. For the liftoff process, 900 nm thick positive photoresist SC1813 is spun and patterned as a sacrificial layer. A thin sacrificial layer is desired for the easier liftoff process. Oxygen plasma cleaning should be avoided before the catalytic metal deposition since it makes the silicon nitride layer more



hydrophilic, thus HF solution attacking the passivation nitride layer and lifting the catalytic metal layer during the final release step.

Two types of catalytic metals, copper and nickel, are evaporated with a 10 nm thick chromium adhesion layer. The thickness of a catalytic metal layer is measured as 312 nm for the copper device and 326 nm for the nickel device. For the metal liftoff, a sacrificial layer is removed with an overnight acetone soak. Figure 3.3 shows the removal of the metal sidewalls after the liftoff process with a 2 minute sonication clean.



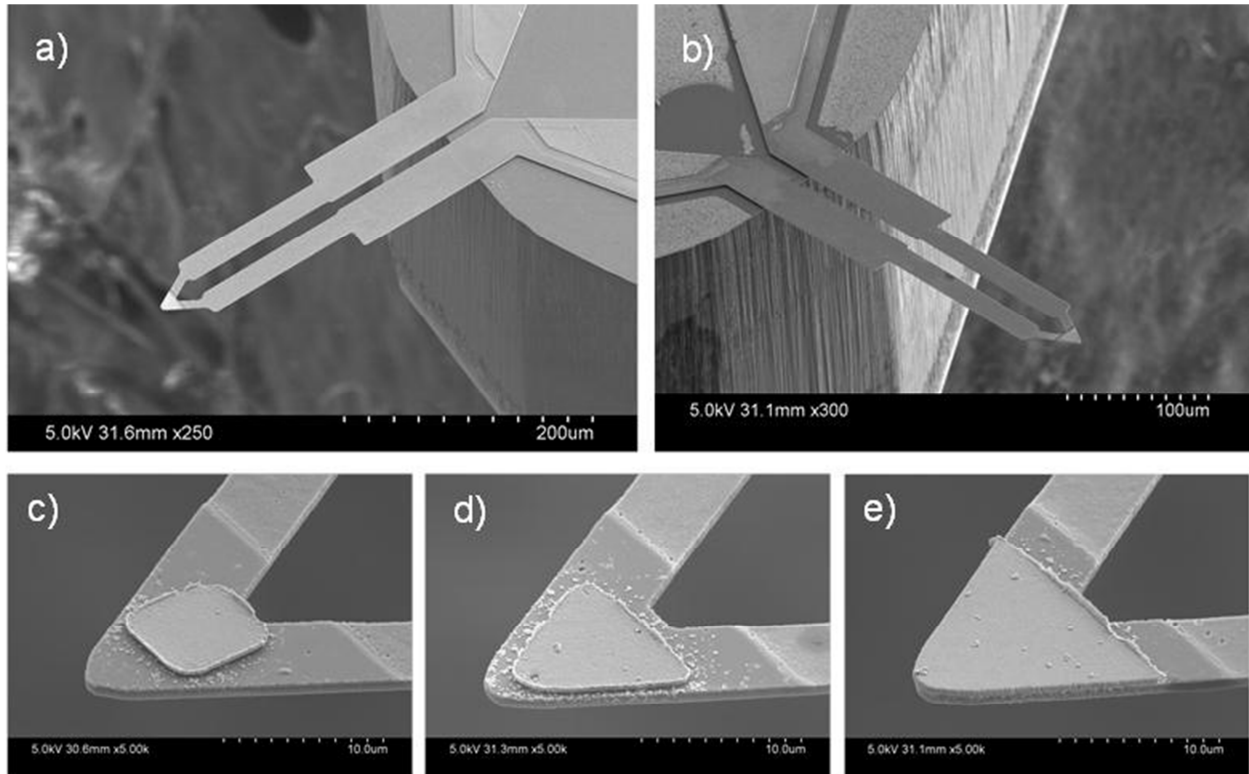
**Figure 3.3** A patterned evaporated nickel layer after the liftoff process. a) The presence of a sidewall right after the metal liftoff. b) A sidewall is removed after 2 minutes of sonication.

### 3.5 Through Wafer Etch and Release

At this point, the device is electrically active and ready for the release. Before the backside photolithography, a 400 nm thick PECVD oxide layer is deposited and an additional 2.7 μm thick SC1827 photoresist layer is spun on the device layer for the cantilever protection. Natural oxides on the backside of a wafer is quickly removed with 5 second BOE etch. Due to the poor etch uniformity of BOSCH process, a wafer is cleaved into four quarters and released separately. A 17 μm thick NR5-800 negative photoresist layer is used for the backside etching

process with its high durability against the lengthy anisotropic silicon etching. Once the backside is patterned with a thick layer of photoresist, the quarter wafer is transferred to a carrier wafer using a NR5-800 photoresist film as an adhesion layer.

To etch the 400  $\mu\text{m}$  thick silicon handle layer, more than 3 hours of ICP-DRIE BOSCH process is needed. Once the buried oxide layer is exposed and the cantilever structure is visible through an etched silicon window, the quarter wafer is placed into 1165 photoresist stripper for more than 12 hours. After separating the quarter wafer from a carrier wafer, a 40 second HF wet etching step removes the oxide layer under the cantilever structure. The presence of the unwanted oxide layer under the cantilever can be detected by checking the cantilever bending. Figure 3.4 shows the released microcantilever heater with three different catalytic metal areas.

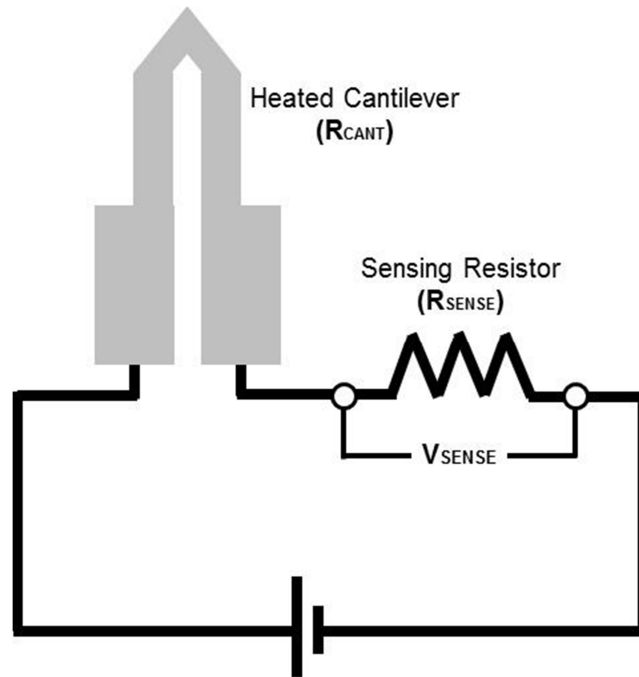


**Figure 3.4** SEM images of the released microcantilever heater. a) The microcantilever heater with a nickel layer. b) The microcantilever heater with a copper layer. c) 5 by 5  $\mu\text{m}$  catalytic metal. d) 14 by 10  $\mu\text{m}$  catalytic metal. e) 20 by 12  $\mu\text{m}$  catalytic metal.

## CHAPTER 4

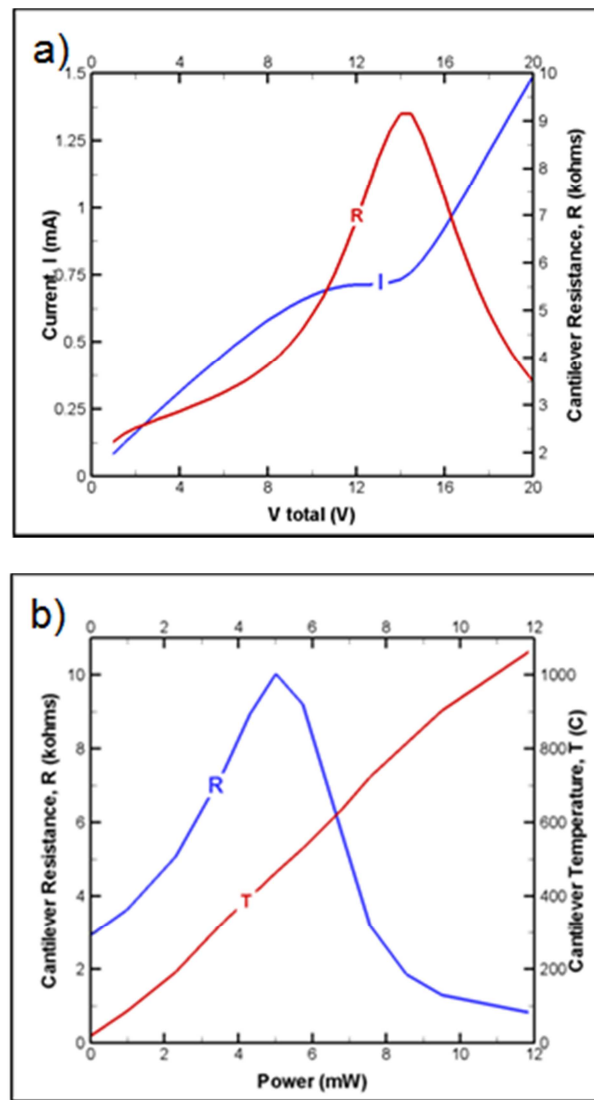
### DEVICE CHARACTERIZATION

Electrical and thermal characterizations are performed on the fabricated microcantilever heater. The microcantilever heater intrinsic resistance values range from 2.8 to 3.9 k $\Omega$ . The resistance values are different among devices due to non-uniform device thicknesses. The device resistivity value is temperature dependent and can be monitored by measuring the voltage across the sense resistor. Figure 4.1 shows a circuit schematic that is used for the device IV characterization. Throughout the entire characterization process, a 10 k $\Omega$  sense resistor is used.



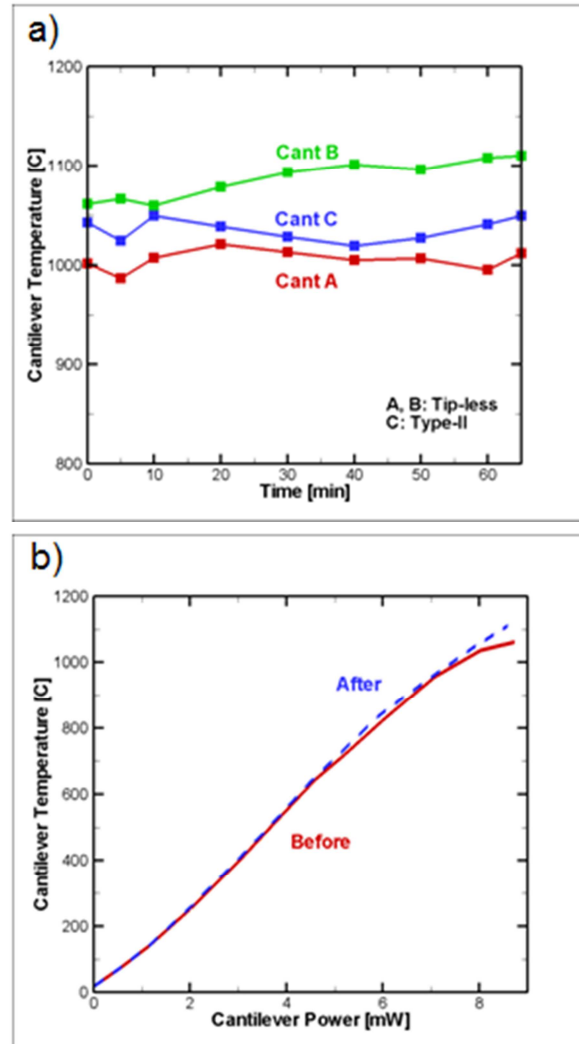
**Figure 4.1** The microcantilever heater / sense resistor circuit for the device characterization. By measuring the voltage across the sense resistor, a current through the entire circuit and the corresponding heater resistance is determined. The power from the microcantilever heater can be calculated with the measured current and the cantilever resistance values.

An operating temperature of the microcantilever heater is measured with Raman spectroscopy, which is an optical measurement technique well suited for the temperature and stress measurements of silicon devices [20]. Temperatures of the microcantilever heater are measured under different input voltage values. At thermal runaway, the microcantilever heater reaches 570°C. The measured temperature at thermal runaway falls into the theoretical thermal runaway temperature range, which is typically 500-600°C [15]. Figure 4.2 shows both electrical and thermal characterization results of the fabricated microcantilever heater.

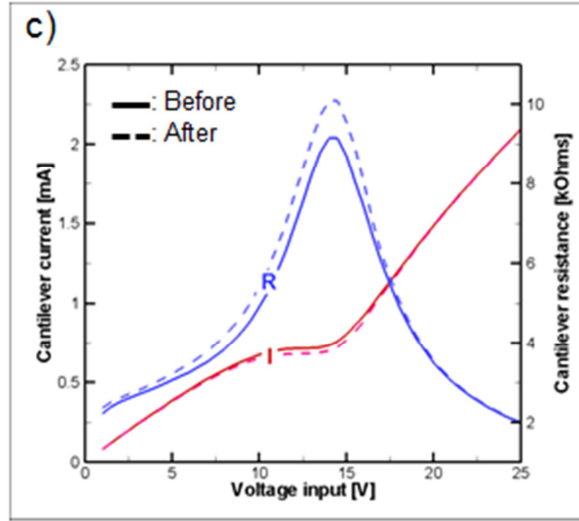


**Figure 4.2** Electrical and thermal characterization results of the microcantilever heater. (a) The IV characterization of the device. (b) The thermal characterization of the device.

A lengthy thermal annealing at 1000°C prior to the CVD graphene growth is required for the natural oxide removal and the larger grain size [8, 10]. The annealing duration ranges from 20 minutes to 1 hour. To determine the adequate annealing period for the microcantilever heater, the device durability is tested. The heated cantilever is maintained at different temperatures for 60 minutes and the heater temperature is measured every 10 minutes. Figure 4.3 shows that the cantilever is still fully operational after the one hour heating at 1000°C. The IV characterization results before and after the testing show that the device resistance slightly increased, which is due to the native oxide formation and the dopant evaporation.

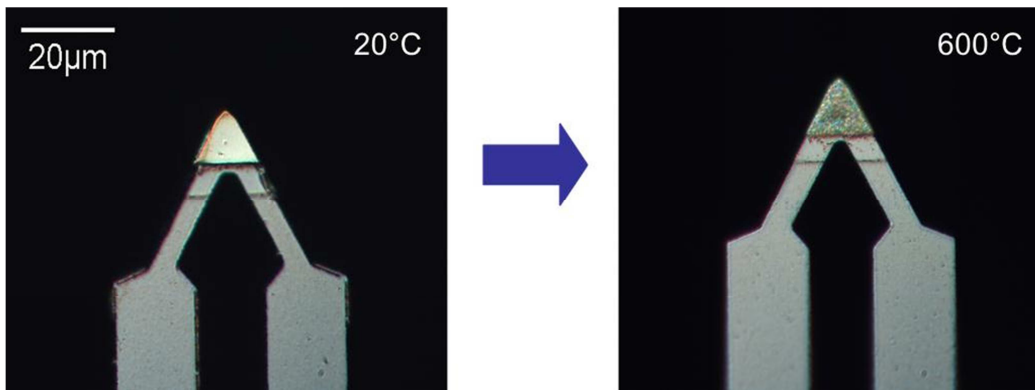


**Figure 4.3** (cont. on next page)



**Figure 4.3** The result of the microcantilever durability study. a) The cantilever temperature as a function of the heating time under different voltage inputs. b) Before and after comparison of the heated cantilever temperature vs. cantilever power. c) The IV characterization comparison before and after the 1 hour heating at 1000°C.

Figure 4.4 shows the degradation of a nickel catalytic layer at 600°C. The nickel started to oxidize at 400°C, which is the known oxidation temperature of nickel [21]. The oxidation of a nickel layer indicates that the cantilever heater region and the catalytic metal are isothermal. Due to the thermal oxidation, the cantilevers with a nickel layer were calibrated up to 300°C before the graphene growth. For the copper patterned cantilevers, the temperature calibration was performed only up to 150°C to prevent the thermal oxidation.



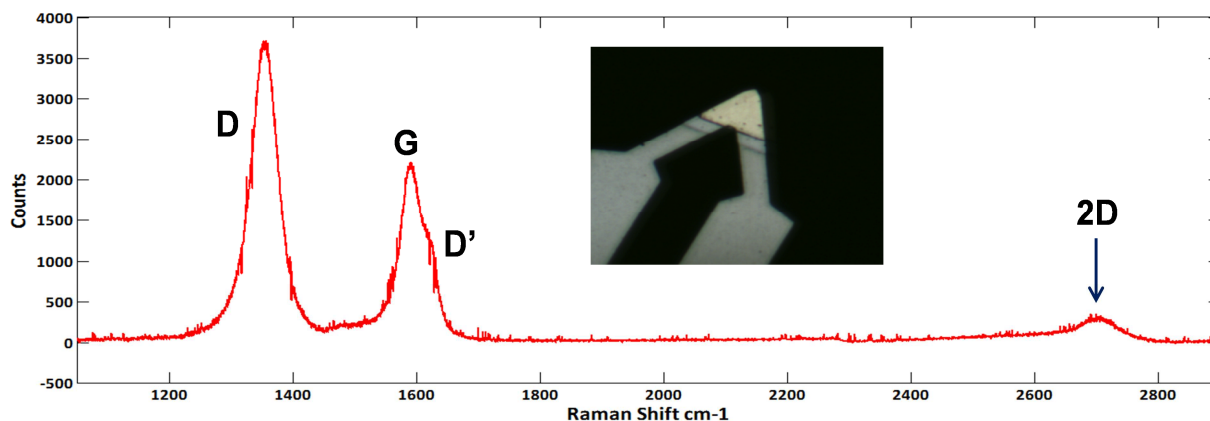
**Figure 4.4** Thermal oxidation of a nickel catalytic metal layer at the heater temperature of 600°C.

## CHAPTER 5

### EXPERIMENT RESULT AND CONCLUSION

#### 5.1 Experiment Result

The CVD growth of a multilayer graphene is carried out on the microcantilever heater with a nickel catalytic metal layer at ambient pressure under the flow of 500 sccm argon, 400 sccm hydrogen, and 2 sccm acetylene at 900°C with 120s growth time. Both the higher acetylene flow rate and the longer synthesis time gave the formation of graphite rather than graphene. Raman spectroscopy is one of standard methods to characterize graphene [22, 23]. Figure 5.1 shows the Raman spectra obtained from a multilayer graphene on the microcantilever heater. The large ratio of G-peak to 2D-peak indicates that the synthesized graphene is multi-layered. A strong D-peak shows the presence of defects on grown graphene. Raman measurements at different locations were identical, meaning the uniform graphene growth. With rapid heating and cooling rates of the microcantilever heater, the entire graphene growth procedure took less than 11 minutes, which is more than 90 % improvement from the conventional CVD graphene synthesis time of 2-3.5 hours.



**Figure 5.1** Raman spectra obtained from a multi-layer graphene on the microcantilever heater.

## 5.2 Future Work

At the moment, there is no recipe established for the monolayer graphene synthesis for both copper and nickel devices. To get a good control over the number of grown graphene layers, the recipe optimization is a must. Once the reliable recipes are built, the design of the single leg microcantilever heater can be applied to build the microcantilever heater arrays. With the microcantilever heater arrays, many different synthesis conditions can be tested simultaneously, which will help understanding the chemistry of the graphene CVD growth.

Growth of graphene from solid carbon sources can be studied using the designed microcantilever heater as well. Recently, a graphene growth method using solid carbon sources has been developed using both copper and nickel substrates [24]. Using solid carbon sources, there is no need of hydrocarbon gas inside the CVD furnace, thus cost effective and easy to reproduce. The rapid heating rate of the microcantilever heater will reduce the damage of a solid carbon source during the heating compared to the conventional CVD graphene synthesis method.

## 5. 3 Summary

In summary, the microcantilever heater with the catalytic metal layer is designed and fabricated for rapid CVD graphene synthesis. The cantilever is capable of operating at the graphene synthesis temperature for longer than an hour. With the nickel device, multi-layer graphene is grown at the atmospheric pressure using acetylene as a hydrocarbon feedstock. The higher flow rate of acetylene and the longer synthesis time grown graphite rather than graphene. Raman spectra indicate that uniform multi-layer graphene is formed over a 20 by 12  $\mu\text{m}$  nickel substrate. The entire graphene growth with the microcantilever heater took 11 minutes, which is reduced by 90% from the conventional CVD graphene synthesis process.



## APPENDIX A

# Graphene Cantilever Fabrication Process

### 0. Wafer Material

Wafer specification: SOI Wafer <100>, Diameter: 100mm (or 4 inch)

Device layer thickness :  $5 \pm 0.5 \mu\text{m}$ , Resistivity: 1-10 Ohm\*cm, Doping: N/Ph

Handle thickness: 500 $\mu\text{m}$ , Handle Resistivity: 1-10 Ohm\*cm, Doping: N/Ph

Box layer thickness: 1 $\mu\text{m}$

Dehydration bake: temperature >120°C, time > 5min

Spin deceleration: less than 1000rpm/sec

### 1. Cantilever formation

#### 1.1 Wafer thinning

**Equipment:** Oxidation Tube

**Equipment:** Oxidation Furnace (MMS)

**Recipe:** Furnace - 1000 °C, 48 Hours, Gas: O<sub>2</sub>, flow rate: 6 sccm

Note: Continue oxidation until silicon layer is 1.5  $\mu\text{m}$  thick

#### 1.2 Spin photoresist (NR7-1500P)

**Equipment:** Spinner

**Recipe:** dehydration bake

Spin NR7-1500P at 1000rpm for 45sec (acceleration 200rpm/sec)

Softbake - 150°C for 1.5min without ring, (or 2 min with ring)

Thickness = ~2.7  $\mu\text{m}$

#### 1.3 Photolithography of Mask #2 (Beam Structure)

**Equipment:** EV420 (MMS)

**Mode:** hard contact

Expose: 25sec

Post-exposure bake: 100°C for 1 min without ring

Development: RD-6, 40sec

Rinse with DI Water and dry w/ N-gun

Note: Alignment is very important. We use **10X** lens in this step. Be very careful during the lens changing process.

#### 1.4 Hard Bake

**Equipment:** Hot Plate

**Recipe:** 120 °C for 10 min with Al ring

### **1.5 Topside Silicon Etch (Anisotropic)**

**Equipment:** ICP-DRIE (MMS)

**Recipe:** Program Name: bosch-1

Estimated Number of Cycles = 12

Note: you will see the uniform oxide layer exposed,

### **1.6 Wafer clean (Acetone soaked)**

**Equipment:** Solvent Bench

**Recipe:** soaked in Acetone, Time = 10 min

Rinse with DI water and dry with N-gun

### **1.7 Piranha Clean**

**Equipment:** Wet Bench (MMS)

**Recipe:** Piranha Solution ( $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  : 70%:30%) at 120°C

Time = 10 min

Rinse with DI water and dry with N-gun

## **2. Implantation (low dosage)**

### **2.1 Spin photoresist (Shipley 1827)**

**Equipment:** Spinner (MMS)

**Recipe:** dehydration bake

Spin Shipley 1827 at 3000rpm for 45sec (acceleration 300rpm/sec)

Softbake: hotplate 120°C for 1.5min without ring, or 2min with ring

Thickness = ~3  $\mu\text{m}$

### **2.2 Photolithography of Mask #3 (Low Dose Implantation)**

**Equipment:** EV420 (MMS)

**Recipe:** *Hard contact mode*

Expose: around 20 sec

*Development:* MF319, around 55 sec

Rinse with DI Water and dry w/ N-gun Note: 4X lens or 10X lens

### **2.3 Hard Bake**

**Equipment:** Hot Plate (MMS)

**Recipe:** 120 °C for 25 min with ring

### **2.4 Ion Implantation of Entire Beam (low dosage)**

**Equipment:** Outside Vendor - Core Systems, CA 3.2.3

**Recipe:** Phosphorus /2.51e13 atoms/cm<sup>2</sup> / 200 KeV/tilt 7°

### **2.5 Photoresist stripping**

**Equipment:** Solvent Bench (MMS)

**Recipe:** soak in Acetone for 10min

## **2.6 Piranha Clean**

**Equipment:** Acid Bench (MMS)

**Recipe:** Piranha Solution ( $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  : 70%:30%)

Time = 10 min

Rinse with DI water and dry with N-gun

## **2.7 Oxide Deposition**

**Equipment:** PlasmaLab PECVD (MNTL)

**Recipe:** high deposition rate

Thickness: 300nm

Time: 12 min

## **2.8 Diffusion**

**Equipment:** Anneal Furnace (MMS)

**Recipe:** Furnace - 1000 °C, 0.5 Hour

$\text{N}_2$  flow at 2 sccm

## **2.9 BOE**

**Equipment:** Wet Bench

**Recipe:** BOE

Time = ~3min (until oxide is fully removed, check the edge surface change from hydrophilic to hydrophobic, then give 30 sec more)

# **3. Implantation (high dosage)**

## **3.1 Shipley 1827**

**Equipment:** Spinner

**Recipe:** dehydration bake

Spin Shipley 1827 at 3000rpm for 45sec (acceleration 300rpm/sec)

Softbake: hotplate 120°C for 1.5min without Al ring , or 2min with Al ring

Thickness = ~3µm

## **3.2 Photolithography of Mask #4 (High Dose Implantation)**

**Equipment:** EV420 (MMS)

**Recipe:** *Exposure*

Hard contact mode

Expose: around 20 sec

*Development: MF319, around 55sec*

Rinse with DI Water and dry w/ N-gun

Note: 4X or 10X lens

## **3.3 Hard Bake**

**Equipment:** Hot Plate

**Recipe:** 120 °C for 25 min with ring

### **3.4 Ion Implantation (high dosage)**

**Equipment:** Outside Vendor - Core Systems, CA

**Recipe:** Phosphorus / $2.51 \times 10^{16}$  atoms/cm<sup>2</sup> / 200 keV / 45° tilt / Orientation 180°

### **3.5 Photoresist stripping (acetone soaking)**

**Equipment:** solvent bench

**Recipe:** soak the wafer in Acetone at room temperature, overnight  
Then place the wafer in ultrasound cleaner for less than 5 minutes

### **3.6 Photoresist stripping (Piranha Clean)**

**Equipment:** Acid Bench

**Recipe:** Piranha Solution (H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub> : 70%:30%) at 120°C

Time = 10 min

Rinse with DI water and dry with N-gun

### **3.7 Photoresist stripping (Oxygen Plasma)**

**Equipment:** Axic RIE (MMS)

**Recipe:** Program Name: ztdai\_O2

Time: 5 min (5min more if necessary)

### **3.8 Oxide Deposition**

**Equipment:** PlasmaLab PECVD (MNTL)

**Recipe:** high deposition rate

Thickness: 300nm

Time: 12 min

### **3.9 Diffusion**

**Equipment:** Anneal Furnace (MMS)

**Recipe:** Temperature = 1000°C

N<sub>2</sub> flow at 2 sccm    Time = 2 hr

## **4. Via and Metallization**

### **4.1 Shipley 1827**

**Equipment:** Spinner (MMS)

**Recipe:** dehydration bake

Spin Shipley 1827 at 3000rpm for 45sec (acceleration 300rpm/sec)

Softbake: hotplate 120°C for 1.5 min without Al ring, or 2 min with Al ring

Thickness = ~3μm

### **4.2 Photolithography of Mask #5 (Open Vias for Metal Contact)**

**Equipment:** EV420 (MMS)

**Recipe:** *Exposure*

Hard Contact (6 μm separation)

Expose: 20sec  
*Development:* MF319, around 55 sec  
Rinse with DI Water and dry w/ N-gun  
Note: 4X or 10X lens

#### **4.3 Hard Bake**

**Equipment:** Hot Plate  
**Recipe:** 110 °C for 10 min with ring

#### **4.4 Topside Oxide Etch**

**Equipment:** Freon RIE (MNTL)  
**Recipe:**  $CF_4$   
Etch Depth Needed = 300 nm  
Time = 18 min (over etch a little bit)

#### **4.5 BOE dip**

**Equipment:** Acid hood (MMS)  
**Recipe:** *BOE dip for 30 sec*

#### **4.6 Photoresist stripping**

**Equipment:** Solvent Bench (MMS)  
**Recipe:** soak in Acetone for 10min

#### **4.7 Piranha Clean**

**Equipment:** Acid Bench (MMS)  
**Recipe:** Piranha Solution ( $H_2SO_4:H_2O_2$  : 70%:30%) at 120°C  
Time = 10 min  
Rinse with DI water and dry with N-gun

#### **4.8 BOE Dip**

**Equipment:** Acid Bench  
**Recipe:** BOE  
Time = 15 sec

#### **4.9 Topside Aluminum Deposition (Evaporation)**

**Equipment:** Evaporator #3 (MRL)  
**Recipe:** 1.5  $\mu m$  Aluminum

#### **4.10 Spin Shipley 1827**

**Equipment:** Spinner (MMS)  
**Recipe:** dehydration bake  
Spin Shipley 1827 at 3000rpm for 45sec (acceleration 300rpm/sec)  
Softbake: hotplate 120°C for 1.5 min without Al ring, or 2 min with Al ring  
Thickness =  $\sim 3 \mu m$

#### 4.11 Photolithography of Mask #6 (pattern Al)

**Equipment:** EV420 (MMS)

**Recipe:** *Exposure*

Hard contact mode

Expose: **35 sec**

*Development: MF319 around 70sec (can be longer do 50 sec in one bath then transfer to second bath, for total 90-120 seconds)*

*Check in between anchors for PR, continue developing until completely removed—OK to overdevelop*

Rinse with DI Water and dry w/ N-gun

**Note:** 4X or 10X lens, **this step needs to be over-exposed**

\*\*\*HARD BAKE 10 minutes at 120

#### 4.12 Aluminum etch

**Equipment:** Acid Bench

**Recipe:** Aluminum Etchant Type A, at 60°C (heat for ~20 minutes firstly)

Estimated Etch Rate = 3000 Å/min

Time = 4 to 5min ~(6 to 9 minutes)

Note: you will see the shiny Al is remove and the color (blue) of SiO<sub>2</sub> shows up, after Al layer is fully etched, give it 30 sec more etch time

#### 4.13 Photoresist Striping

**Equipment:** Solvent Bench (MMS)

**Recipe:** Soak in Acetone for 10 min

Check Resistance if around 2kohm do not need to sinter  
If greater than 40 or 50 kohm then

#### 4.14 Oxygen Plasma (optional)

**Equipment:** Axic RIE (MMS)

**Recipe:** ztdai\_O2

Time: 3 min

Alternative: Jupiter for 1 min at 250 W

#### 4.15 Check Device Resistance with Multimeter

**Note:** the resistance of type II device is around 2 KOhms

#### 4.16 Sintering

**Equipment:** Vacuum Annealer (MMS)

**Recipe:** Temperature = 400°C Time = 0.5 hr

## 5. Catalytic Metal Deposition

### 5.1 Nitride Deposition

**Equipment:** STS PECVD (MNTL)

**Recipe:** Mixed Frequency

Nitride thickness = 200nm

Time = 14min

Note: this nitride layers is passivation layer

### 5.2 Shipley 1813

**Equipment:** Spinner (MMS)

**Recipe:** dehydration bake

Spin Shipley 1813 at 3000rpm for 45sec (acceleration 300rpm/sec)

Softbake: hotplate 120°C for 1.5 min without Al ring, or 2 min with Al ring

Thickness = ~3µm

### 5.3 Photolithography of Mask #8 (Catalytic metal patterning)

**Equipment:** EV420 (MMS)

**Recipe:** *Exposure*

Hard Contact (6 µm separation)

Expose: 20sec

*Development:* MF319, around 55 sec

Rinse with DI Water and dry w/ N-gun

Note: 4X or 10X lens

### 5.4 Catalytic Metal Deposition (Evaporation)

**Equipment:** Evaporator #2 (MRL)

**Recipe:** 10 nm Chrome + 300 nm Copper (or Nickel)

### 5.5 Metal Liftoff

**Equipment:** Wet Bench

**Recipe:** soak the wafer in Acetone at room temperature, overnight

Then place the wafer in ultrasound cleaner for less than 5 minutes

Note: Check with SEM to make sure there is no side-walls

### 5.6 Oxide Deposition

**Equipment:** Plasma PECVD (MNTL)

**Recipe:** High deposition rate

Oxide thickness = 400nm

Time = 16min

Note: this layer of Oxide just to keep the final device clean

## 6. Cantilever Release

### 6.1 Apply Thick Photoresist (PR) to Topside

**Equipment:** Spinner (MMS)

**Recipe:** dehydration bake

Spin Shipley 1827 at 3000rpm for 45sec (acceleration 300rpm/sec)

Softbake: hotplate 120°C for 1.5 min without Al ring, or 2 min with Al ring

Thickness = ~3  $\mu\text{m}$

### 6.2 Hard Bake

**Equipment:** Hot Plate 3.2.5

**Recipe:** 110 °C for 10 min

### 6.3 BOE Dip

**Equipment:** Acid Bench (MMS)

**Recipe:** BOE

Time: 10 sec, until oxide on the back side is fully removed

### 6.4 Cleave Wafer

**Equipment:** Work Bench

**Recipe:** Cleave wafer into 4 quadrants

### 6.5 Apply Thick Photoresist (PR) to Bottomside

**Equipment:** Spinner (MMS)

**Recipe:** dehydration bake

Spin NR5-8000 at 1000rpm for 40sec (acceleration 200rpm/sec)

Softbake: 150°C for 6min

Thickness = ~ 17  $\mu\text{m}$

Note: cover the hotplate with aluminum foil to avoid leaving photoresist residue on the hotplate. Cool down on Alphawipe before exposed in EV420

### 6.6 Photolithography of Mask #7 (Backside Openings)

**Equipment:** EV420 MMS)

**Recipe:** *Exposure*

Hard Contact Mode or proximity mode (50um of separation)

Time = 30 sec

Post exposure bake: 100°C for 2min

*Development: RD-6, around 70 sec*

Rinse with DI Water and dry w/ N-gun

Note: use default backside alignment lens

### 6.7 Hard Bake

**Equipment:** Hot Plate (covered with Al foil)

**Recipe:** 120 °C for 10 min

### 6.8 Apply Thick Photoresist (PR) to Topside of Carrier Wafer



**Equipment:** Spinner (MMS)

**Recipe:** dehydration bake

Spin NR5-8000 at 1000rpm for 40sec (acceleration 200rpm/sec)

#### **6.9 Attach 1/4 Wafer to Carrier Wafer**

**Equipment:** By Hand

**Recipe:** N/A

#### **6.10 Hard Bake**

**Equipment:** Hot Plate (MMS)

**Recipe:** 120 °C for 10 min, 140 °C for 20 min with Al ring

#### **6.11 Backside Silicon Etch**

**Equipment:** ICP-DRIE (MMS)

**Recipe:** Bosh-1

Estimated Number of Cycles = 800

Note: you will see the cantilever structure from the etched trench, the 1 μm thick box SiO<sub>2</sub> layer is transparent

#### **6.12 Soak to Separate Wafers**

**Equipment:** Wet Bench

**Recipe:** Photoresist Stripper 1165 at 80C°

Time = overnight

#### **6.13 Wafer clean (optional, for dirty quadrants)**

**Equipment:** Acid Bench (MMS)

**Recipe:** Piranha Solution (H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub> : 70%:30%)

Temperature: 120C°      Time = 5 sec

Rinse in DI water and change DI water 5 times, then dry on a hot plate at 110C°.

**After this step, we can't clean the wafer with DI water gun and dry the wafer with N<sub>2</sub> gun.**

#### **6.14 HF Dip**

**Equipment:** Wet Bench 3.2.5

**Recipe:** HF 49%

Box oxide Thickness = 1 μm      Time = around 40 sec

Rinse in DI water and change DI water 5 times, then dry on a hot plate at 110C°

Note: check devices under optical microscope to see cantilevers are not bending, use multi-meter to check device resistance.

#### **6.14 Device final check (SEM)**

**Equipment:** Hitachi SEM S4800 (MNTL)

**Recipe:** N/A

Final check

## APPENDIX B

### CANTILEVER OPERATION UNDER DIFFERENT CIRCUMSTANCES

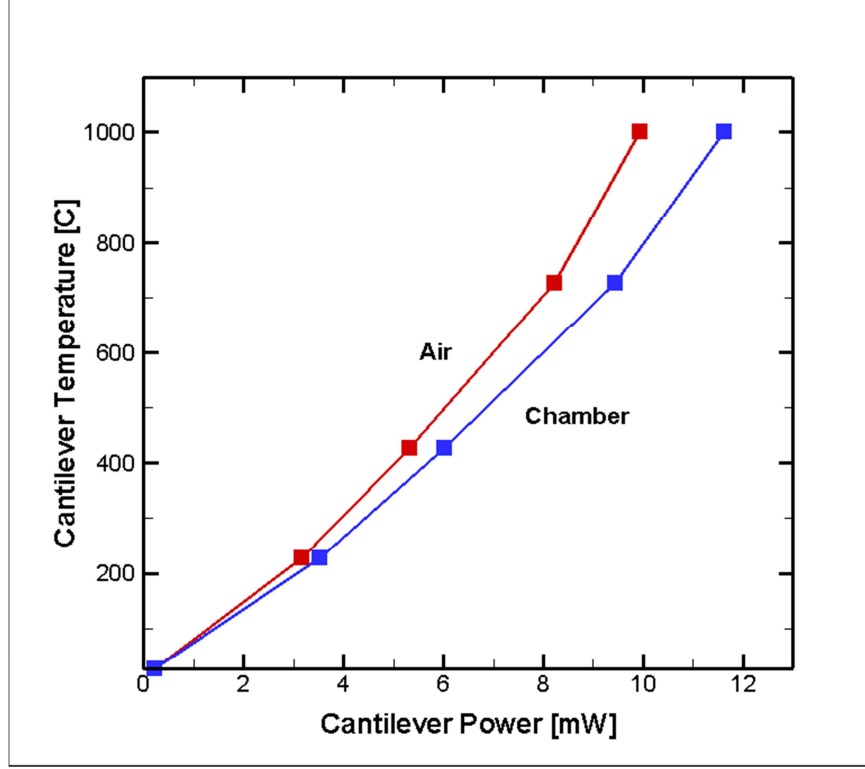
Simple calculations are conducted to understand the microcantilever heater behavior under different circumstances. First, the effect of the gas mixture for the CVD graphene growth is studied. Since the composition of the gas mixture during the CVD graphene growth is different from air, the thermal conductivity values should be different. The thermal conductivity of the gas mixture inside the CVD furnace has been calculated using the equation B.1 [25], where  $y$  is the mole fraction,  $k$  is the thermal conductivity, and  $M$  is the molecular weight of a gas.

$$k_{mix} = \frac{\sum y_i k_i (M_i)^{1/3}}{\sum y_i (M_i)^{1/3}} \quad (\text{B.1})$$

Table 2.1 shows the gas mixture composition for the conventional CVD graphene synthesis on a nickel substrate. The calculated thermal conductivity of the gas mixture is 0.036 W/mK, which is 40 % higher than that of air. Since the thermal conductivity is higher, more power is dissipated through the gaseous medium during the CVD graphene synthesis. Figure B.1 shows the simulated results of the cantilever temperature as a function of the cantilever power in air and the gas mixture for the CVD graphene growth. As expected, a higher cantilever power is required to achieve the synthesis temperature for the CVD graphene growth.

Gas	Flow rate (sccm)	Thermal conductivity (W/mK)	Molecular weight (g/mol)
Hydrogen (H <sub>2</sub> )	20	0.1805	2
Argon (Ar)	50	0.0172	40
Methane (CH <sub>4</sub> )	35	0.0331	16

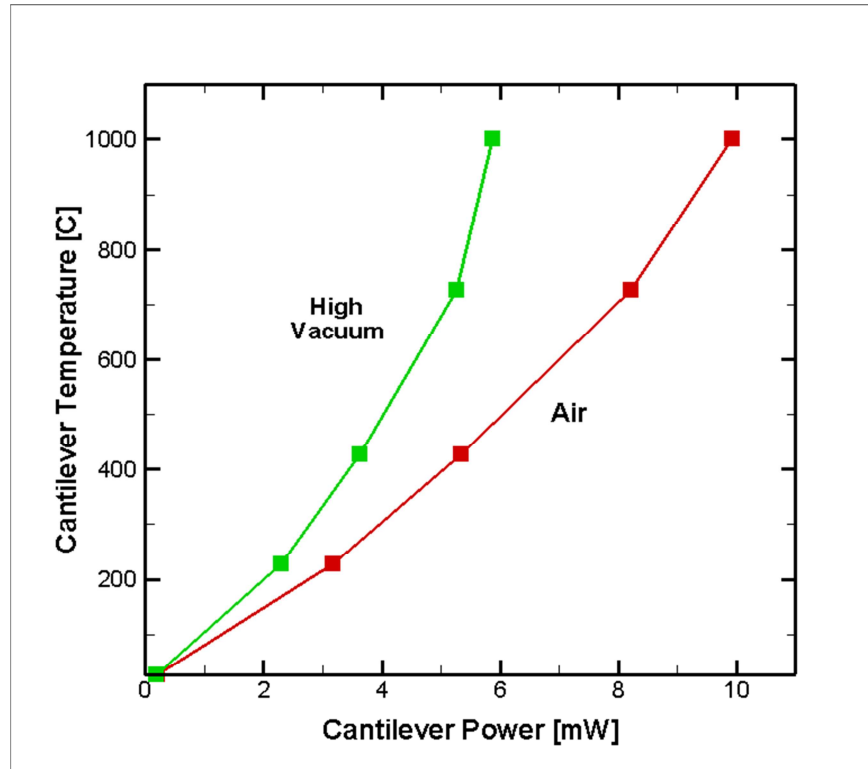
**Table B.1** Flow rate and property of gases for graphene synthesis with nickel substrate



**Figure B.1** A simulated result of the cantilever temperature as a function of the cantilever power under different gas environments

The graphene growth with a copper substrate requires high vacuum throughout the entire process ranging from 0.3 mbar to 0.8 mbar [9, 26]. At high vacuum, the heat transfer between the cantilever and its gaseous surroundings is negligible compared to the thermal conduction through cantilever legs. The Knudsen number,  $Kn = \lambda/l$ , is the ratio of the energy carrier mean free path  $\lambda$  to the size of either the heater or the constriction,  $l$ . The Knudsen number is a good indicator to determine whether the thermal transport through the gaseous surrounding is taking place or not. When the Knudsen number is less than 1, the thermal transport from the cantilever heater to the surrounding gas depends on gas pressure, and when the Knudsen number is larger than 1, the thermal transport from the cantilever heater remains constant [27]. With the negligible thermal transport from the heater to gaseous surrounding, less power is required to reach the synthesis

temperature in high vacuum. Figure B.4 shows the cantilever temperature as a function of the cantilever power at both atmospheric pressure and high vacuum. At high vacuum, 40 % less power is required to reach 1000°C.



**Figure B.2** The cantilever temperature as a function of the cantilever power at both atmospheric pressure and high vacuum.

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